

FIG. 1

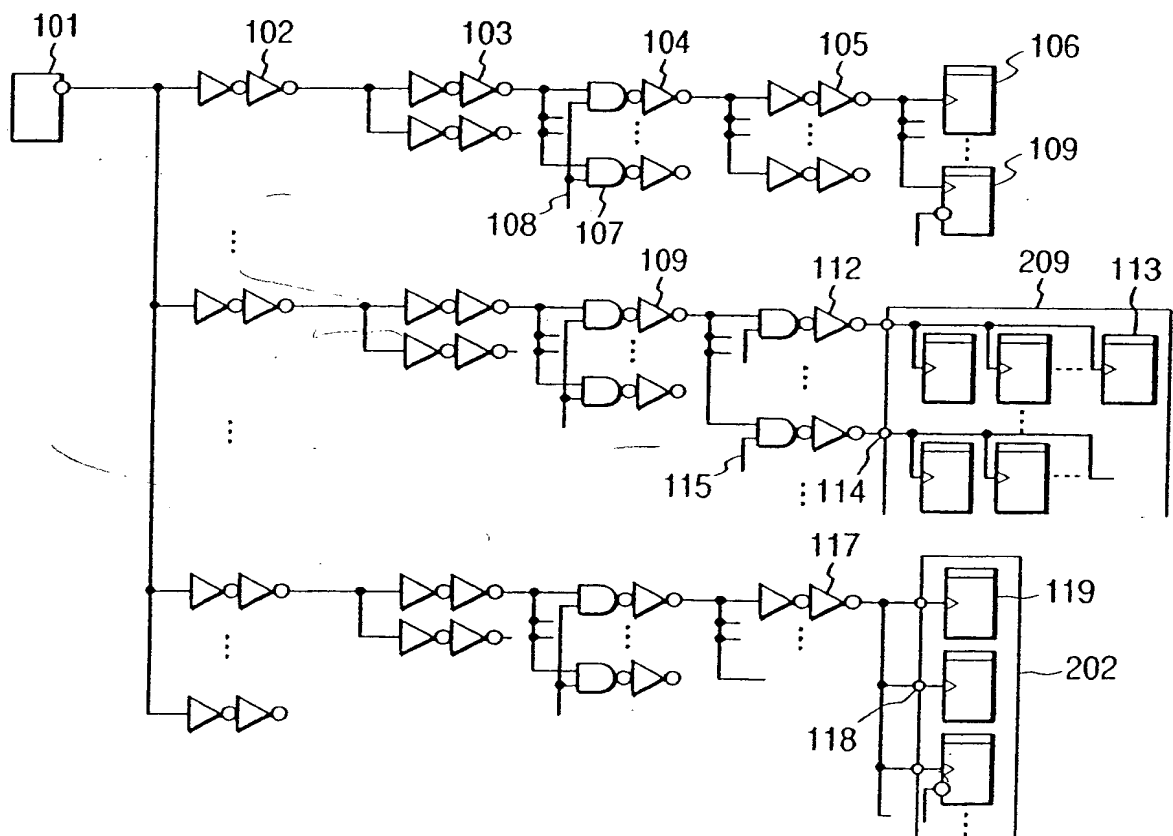


FIG. 2

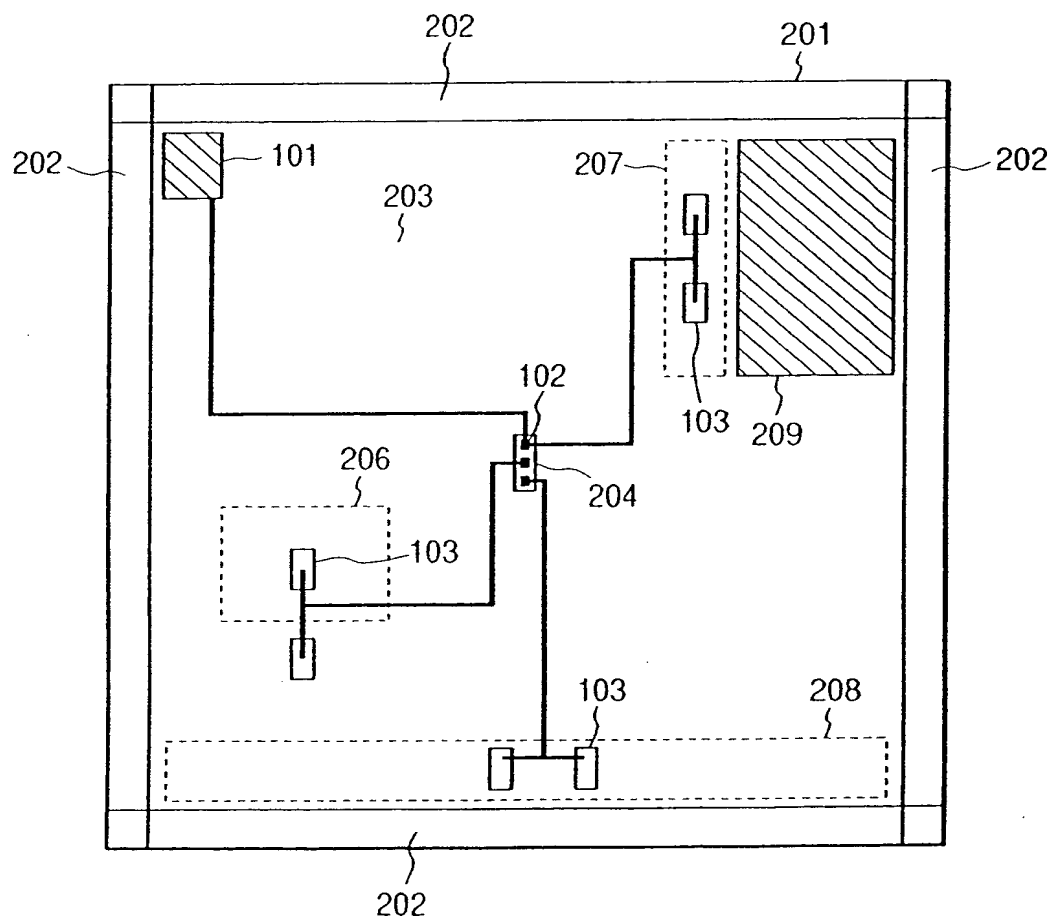


FIG. 3

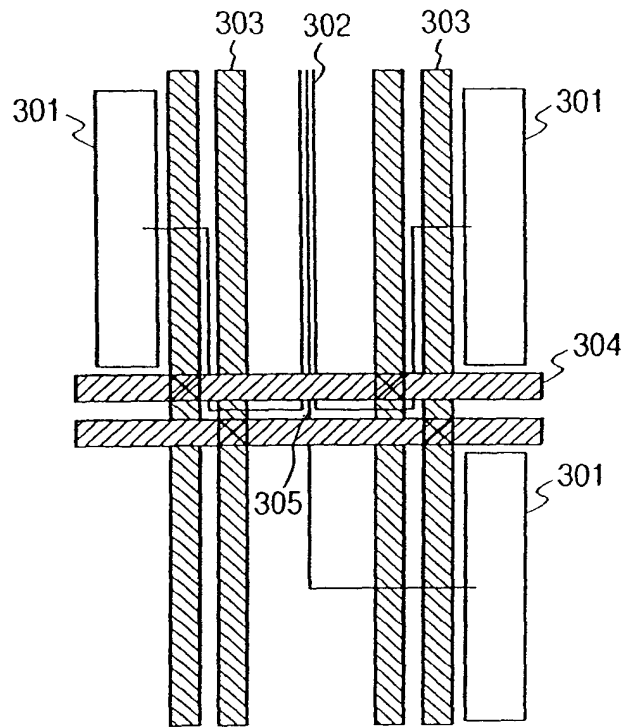


FIG. 4

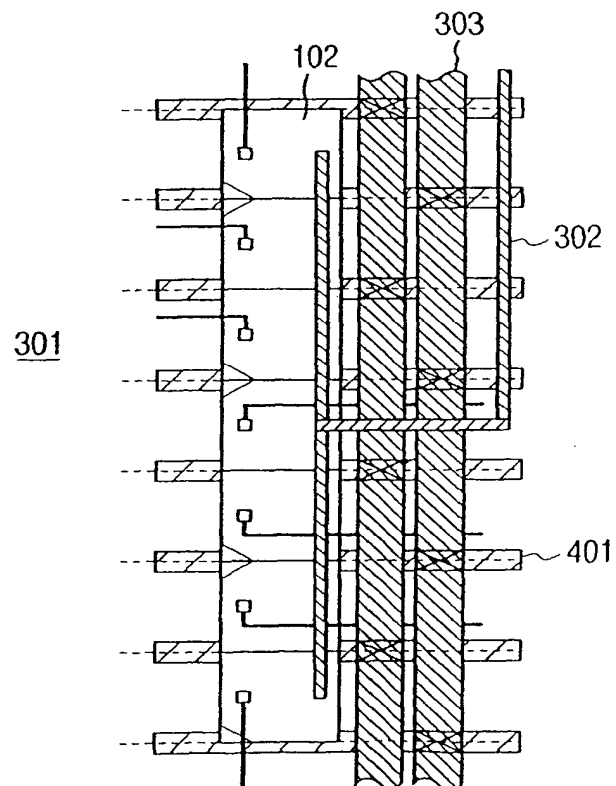


FIG. 5

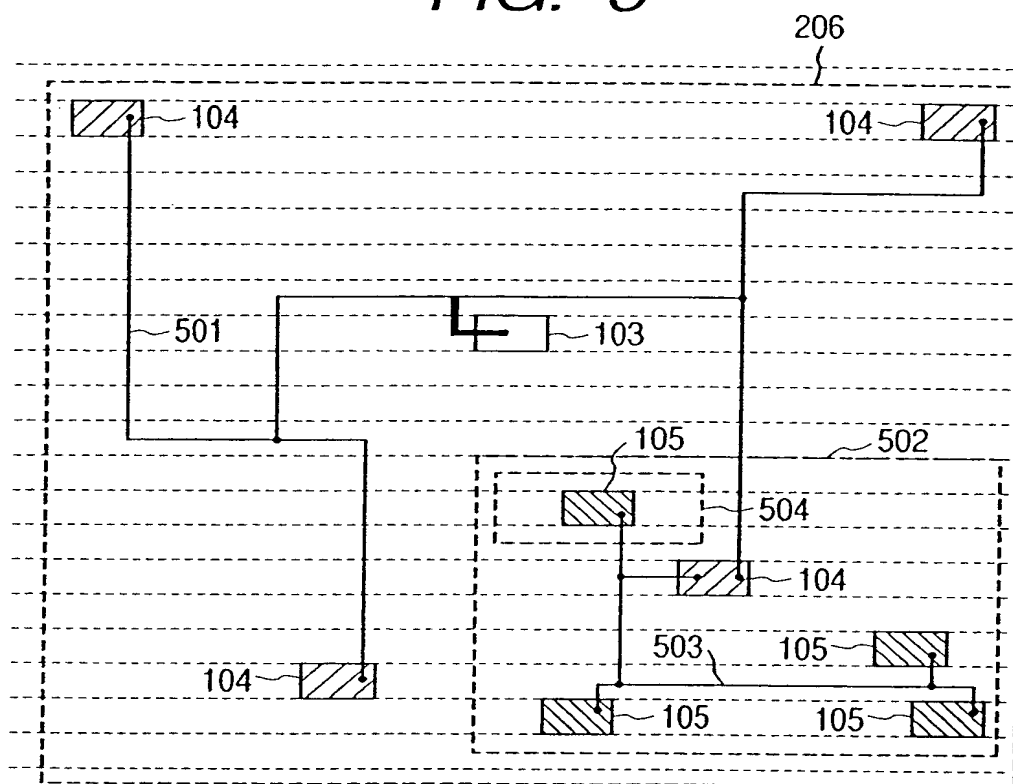


FIG. 6

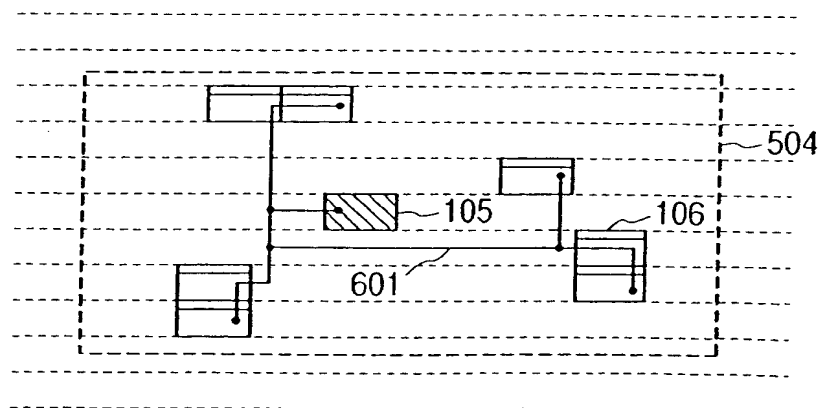


FIG. 7

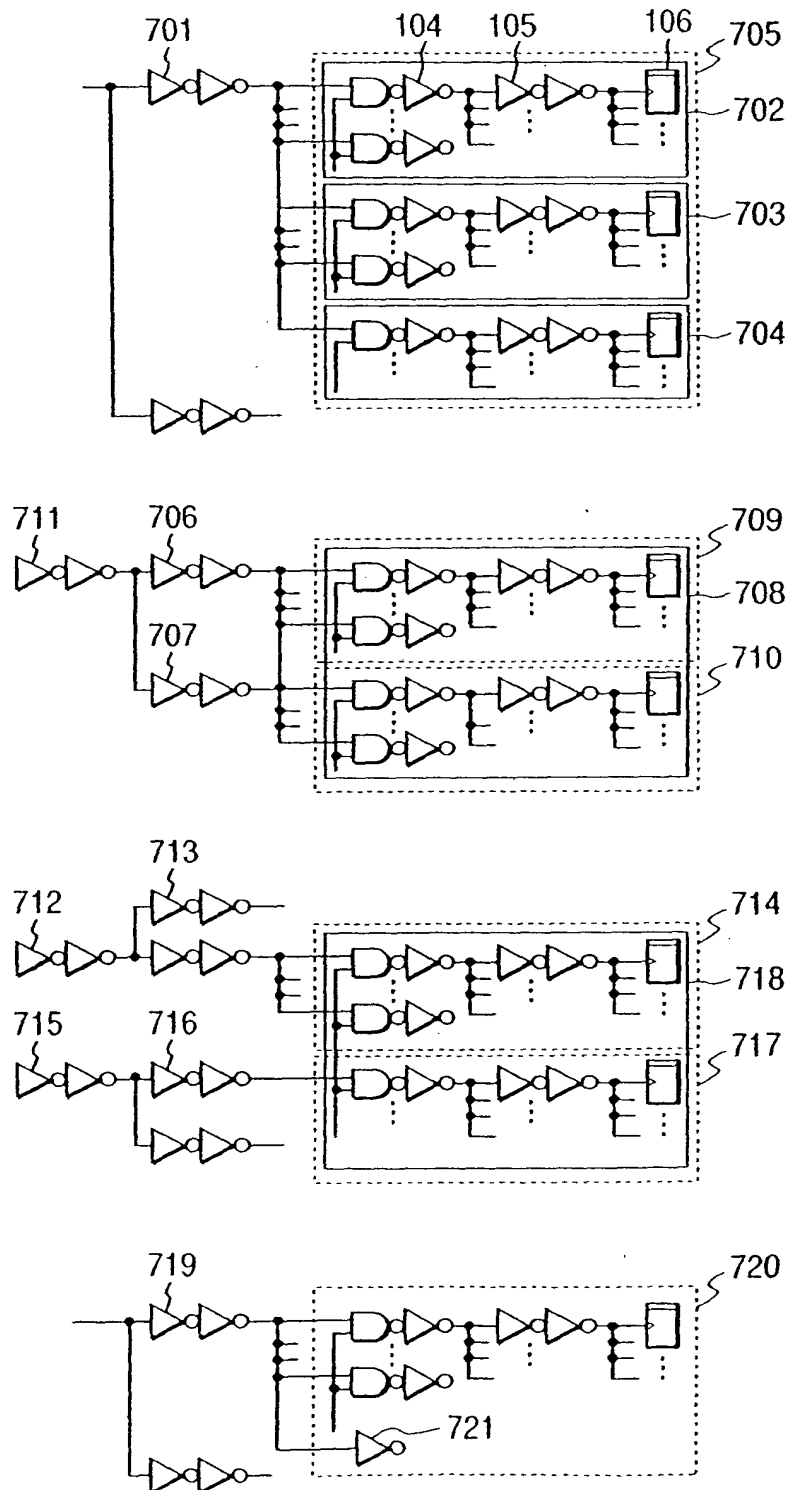


FIG. 8

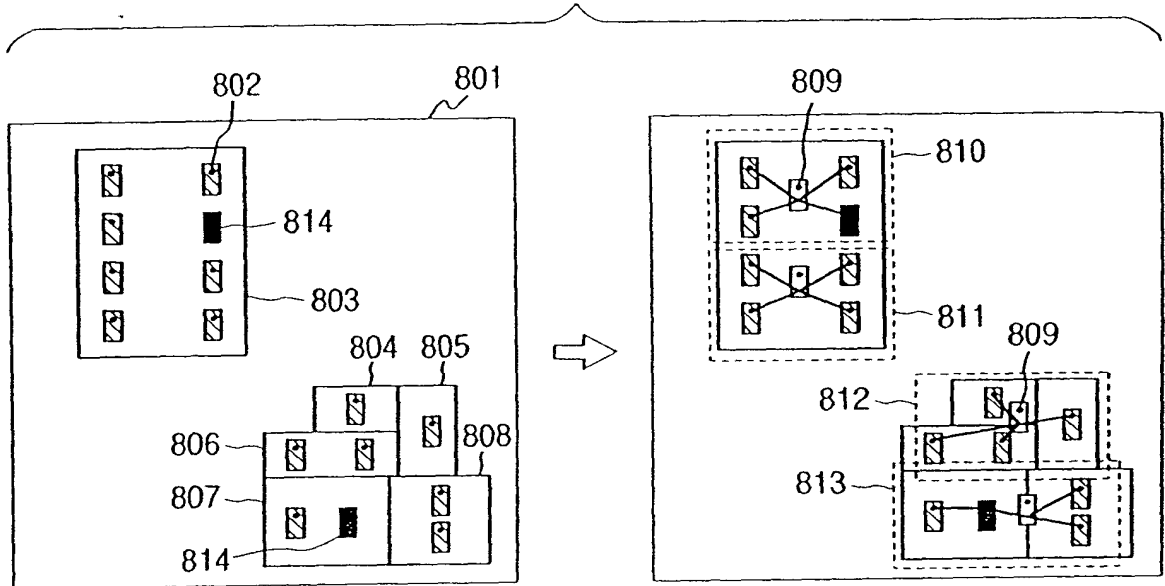


FIG. 9

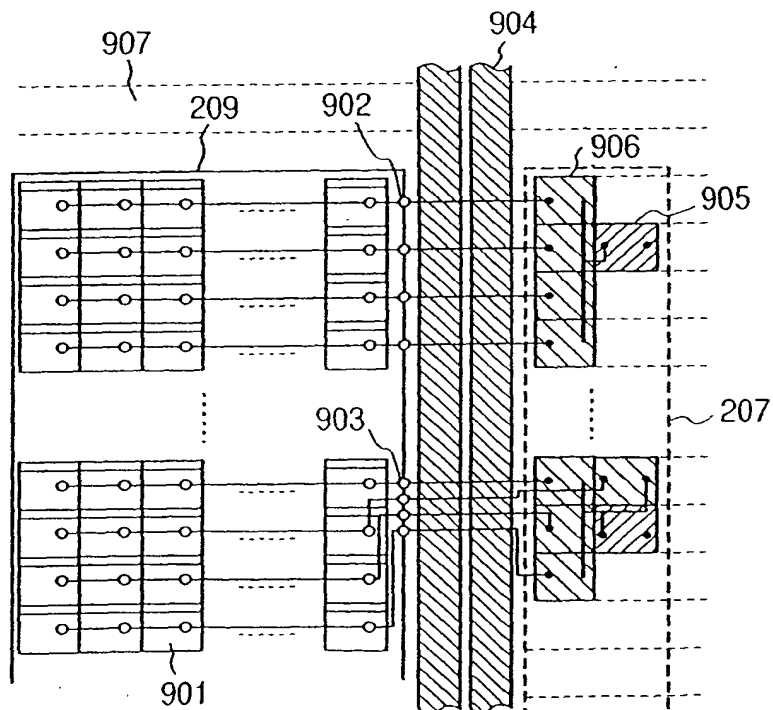


FIG. 10

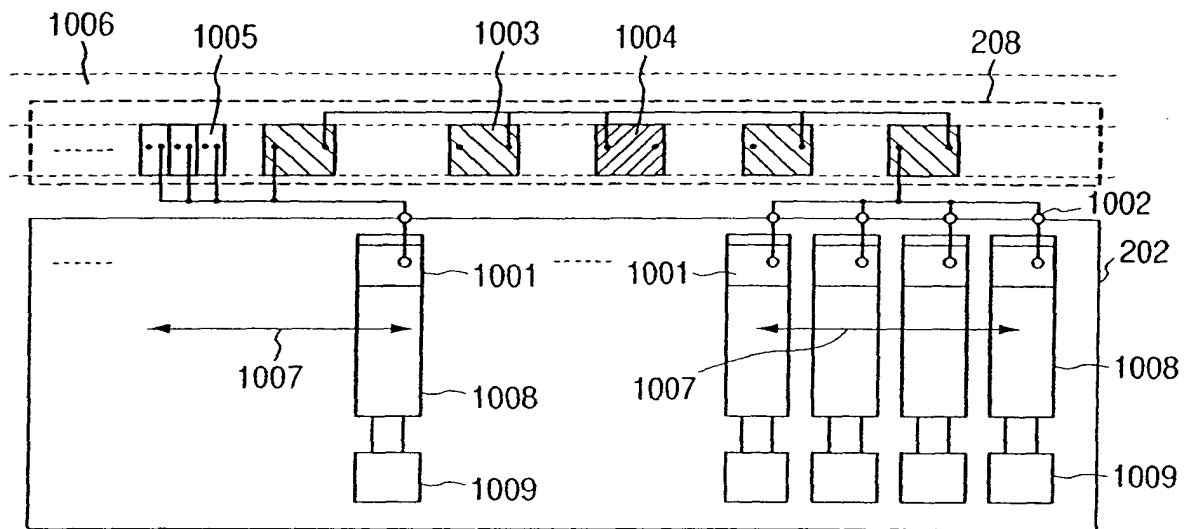


FIG. 11

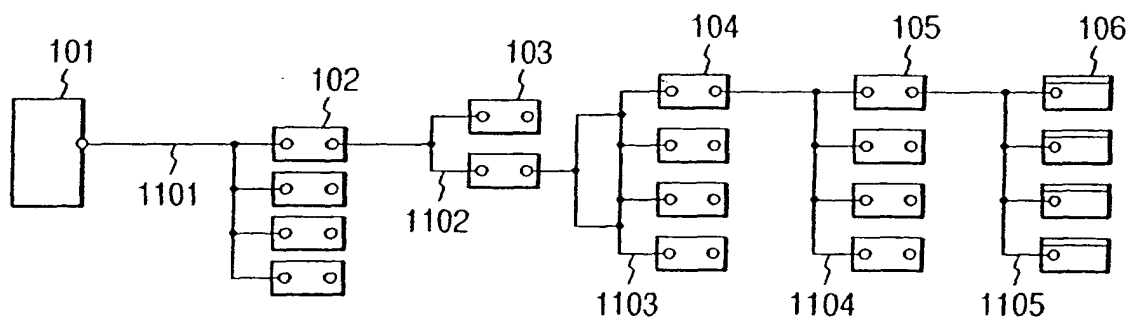


Figure 1 is a schematic diagram of a delay circuit. The top part of the diagram shows a signal path from input 102 through a series of delay elements 1102 and 103, with a total delay indicated by a horizontal arrow labeled "DELAY". The bottom part of the diagram shows a detailed view of the delay elements 102, 1102, and 103, with a signal path 1204 connecting them, and a feedback path 1205 and 1206 connecting the output 103 back to the input 102.

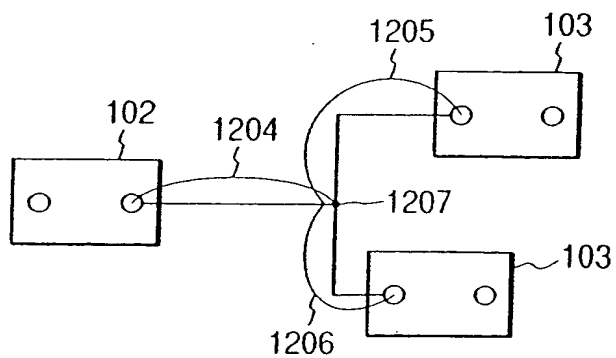




FIG. 13

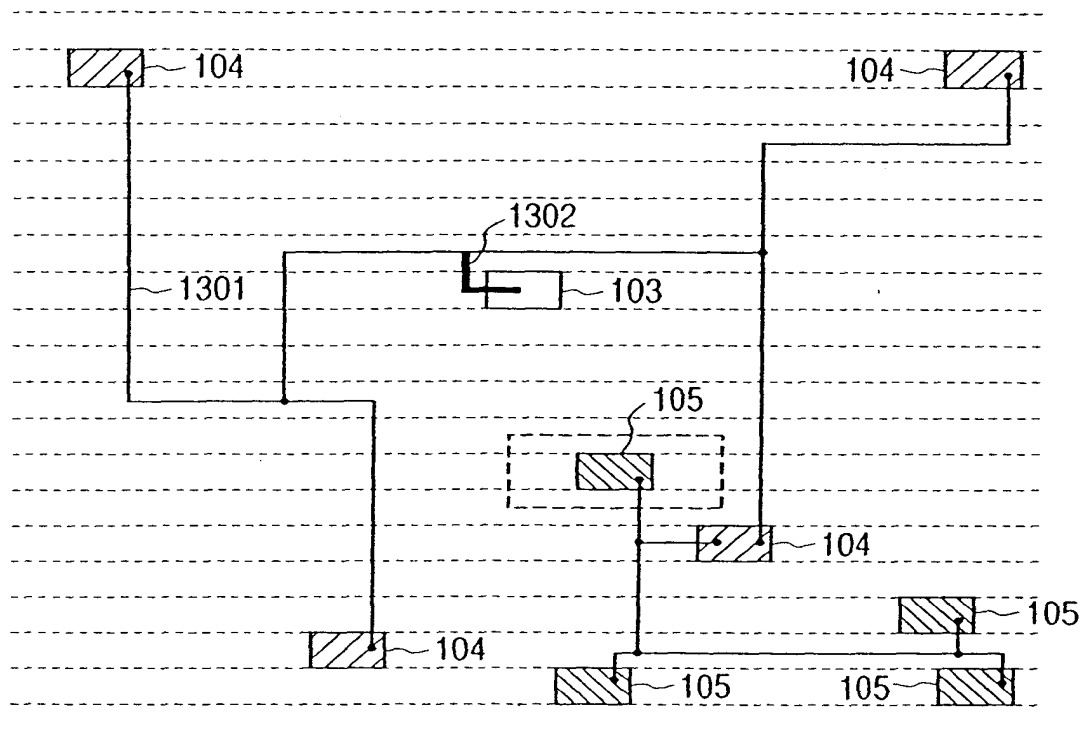


FIG. 14

